UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,780	03/07/2005	John Domokos	2002P00596	6582

24131 7590 01/16/2009
LERNER GREENBERG STEMER LLP
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
HUANG, DAVID S	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
01/16/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/501,780	DOMOKOS, JOHN	
	Examiner	Art Unit	
	DAVID HUANG	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) *8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed 10/23/2008, with respect to the rejection(s) of claim(s) 1, 5, 7, 10, and 15 under non-statutory type obviousness double patenting have been fully considered, but are not persuasive.

Applicant's argument: In contrast to Applicant's invention of claims 1 and 10, claim 14 of the '619 patent does not teach or suggest generating a predistorted RF signal, as particularly claimed by Applicant. Applicant is not claiming that the respective inphase and quadrature signals are respective predistorting coefficients, but rather, that they are combined with respecting predistorting coefficients.

Examiner's response: To clarify the intended meaning of the obviousness type double patenting rejection of 7/23/2008, Examiner notes that the claim language of the present application reproduced in the rejection was altered to better match the wording of the reference patent. That is to say, US '619 identifies "inphase and quadrature signals" output from the signal splitter (claim 4, column 4, lines 59-61). US '619 also identifies an inphase branch or multiplying the signal with inphase signals, and a quadrature branch for multiplying the signal with quadrature signals (claim 11, column 5, line 17 - column 6, line 2). For examination on the merits, "the inphase and quadrature signals" of claim 4 are understood to be different from the inphase and quadrature signals in the respective inphase and quadrature branches of claim 11, which are treated as inphase and quadrature coefficients. Thus, the combination presented below, was not meant to replace the in-phase and quadrature components as recited in claim 1 of

the present application, but to identify the inphase and quadrature coefficients of claim 11 of US '619 as predistortion coefficients.

Applicant's argument: The US '619 patent and Briffa both fail to teach or suggest combining the X2 signal, in-phase and quadrature components, and an external signal with respective predistortion coefficients to generate the predistorted signal, as required by Applicant's claims 1 and 10.

Examiner's response: Applicant argues particularly that US '619 and Briffa teaches multiplying only the X and X^2 signals by the generated coefficients but does not multiply in-phase and quadrature components with respective predistortion coefficients. Examiner notes that Briffa teaches 90° splitter 35 which splits input signal x into two branches and multiplies one branch by 0° and the other by 90°, thereby enabling the QGPA 36 to multiply the complex predistortion signal p from the PreD 37 with the signal x and thereby adjust the magnitude and phase of the signal x (Fig. 2 and 3, column 6, lines 9-17). Both I and Q components of X are sent into QGPA 36, and are multiplied by respective predistortion signals p_i and p_q, as is suggested by the structure of the prior art QGPA (Fig. 2). Each predistortion signal is a polynomial of x, each term multiplied by a respective I or Q coefficient (as defined by Equations 2a and 2b; see column 6, lines 19-40). Therefore, I and Q components are in fact multiplied/combined with respective predistorting coefficients, and the obviousness-type double patenting rejection is properly maintained.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection

is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. **Claims 1, 5, 7, 10 and 15** are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 7,268,619 (hereinafter US '619) in view of Briffa et al. (US 6,075,411).

Regarding **claims 1 and 10**, claim 14 of US '619 discloses a compensating apparatus for compensating for intermodulation products, the apparatus comprising:

a phase splitting unit, which splits an input RF signal into an in-phase component and a quadrature component (column 4, lines 59-61; claim 4);

first multiplying units, which square the value of the in-phase component and the quadrature component respectively (column 4, lines 65-67, claim 5);

a first summer which sums the squared values to generate an X^2 signal (column 5, lines 1-3; claim 6);

combining units, which respectively combine the X^2 signal, the in-phase component, the quadrature component, and an external signal with respective inphase and quadrature signals (column 5, line 17 - column 16, line 2, claim 11); and

an adder, which generates a predistorted RF signal from the output of the combining units (column 6, lines 3-13, claims 12-14).

However, claim 14 of US '619 fails to expressly disclose the combining units respectively combine the X^2 signal, the in-phase component, the quadrature component, and an external signal with respective predistorting coefficients.

Nevertheless, US '619 claims a pre-distorter with multipliers for further multiplying the signal from previous multipliers to generate a further signal, and an inphase branch for multiplying the signal with inphase signals, and a quadrature branch for multiplying the signal with quadrature signals (column 5, lines 11-13, and column 5, line 17-column 6, line 2).

Briffa et al. also discloses a predistortion circuit 37 which generates a complex predistortion signal p which comprises both in-phase and quadrature predistortion coefficients C_0, C_1 and C_2 (see equations 1-4c), each applied to different powers of the input signal x (column 6, lines 13-54, Figs. 3 and 4). Briffa teaches 90° splitter 35 which splits input signal x into two branches and multiplies one branch by 0° and the other by 90°, thereby enabling the QGPA 36 to multiply the complex predistortion signal p from the PreD 37 with the signal x and thereby adjust the magnitude and phase of the signal x (Fig. 2 and 3, column 6, lines 9-17). Both I and Q components of X are sent into QGPA 36, and are multiplied by respective predistortion signals p_i and p_q, as is suggested by the structure of the prior art QGPA (Fig. 2). Each predistortion signal is a polynomial of x, each term multiplied by a respective I or Q coefficient (as defined by Equations 2a and 2b; see column 6, lines 19-40). Thus, the I and Q components are multiplied/combined with respective predistorting coefficients.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to specify the respective inphase and quadrature to be respective predistortion coefficients, since Briffa et al. discloses inphase and quadrature components to predistortion coefficients C0 to C2 (equation 4a-4c) and this increases adaptability by enabling the system to multiply a complex predistortion signal with the input signal to adjust both magnitude and phase (column 6, lines 13-18, Fig. 3).

Regarding **claim 5**, US '619 and Briffa et al. disclose everything claimed as applied to claims 1 and 10 above, but fail to expressly disclose the apparatus is an application specific integrated circuit (ASIC).

However, ASICs are well known in the art to reduce circuit size, decrease performance variations, and reduce the distance between circuit components, as evidenced by Johnson et al. (column 5, lines 25-29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the apparatus as applied to claim 1 as an ASIC since ASICs are well known in the art to reduce circuit size, and decrease performance variations.

Regarding **claims 7 and 15**, US '619 discloses everything claimed as applied to claims 1 and 10 above, and further disclose the apparatus (and method) comprising a further multiplier, which squares the X^2 signal again to give a X^4 signal, wherein the external signal is the X^4 signal (column 5, lines 4-6, claim 7).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-4 and 10-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Briffa et al. (US 6,075,411).

Regarding **claims 1 and 10**, Briffa et al. disclose a compensating apparatus and method for compensating for intermodulation products, the apparatus comprising:

a phase splitting unit, which splits an input RF signal into an in-phase component and a quadrature component (splitter 35, Figure 3);

first multiplying unit, which square the value of the envelope of the RF input to generate an X^2 signal (Squarer 52, Figure 4; column 7, lines 64-65);

combining units, which respectively combine the X^2 signal, the in-phase component, the quadrature component, and an external signal (|x|) with respective predistorting coefficients (multiplier circuits 53-56, Figure 4; QGPA 36, Figure 3; column 7, line 65 - column 8, line 15; column 6, lines 34-39; see also equations 1, 2a, 2b, 3 and 5); and

an adder (summer in QGPA 36, column 6, lines 36-39), which generates a predistorted RF signal from the output of the combining units (column 6, lines 13-25, Figure 3).

Briffa et al. fail to expressly disclose first multiplying units, which square the value of the in-phase component and the quadrature component respectively and a first summer which sums the squared values to generate an X^2 signal.

However, it would have been an obvious matter of design choice to generate the X^2 signal by squaring an in-phase component and a quadrature phase component, respectively, and then summing the squared values since applicant has not disclose that this specific means of

calculation solves any stated problem or is for any particular purpose and it appears that the Squarer 52, taught by Briffa et al., and the claimed first multiplying units and first summer perform equally well in generating the X^2 signal (which is represents magnitude of the input RF signal squared in both the present invention and the prior art reference Briffa et al.)

Regarding **claims 2 and 11**, Briffa et al. disclose everything claimed as applied to claims 1 and 10 above, and further disclose A compensating apparatus according to claim 1, wherein the combining units comprise first to sixth combining units,

the first combination unit combining the X^2 signal with a first predistorting coefficient (multiplier 54, coefficient C2i, Figure 4);

the second combining unit combining the X^2 signal with a second predistorting coefficient (multiplier 56, C2q, Figure 4);

the third combining unit combining the external signal with a third predistorting coefficient (multiplier 53, coefficient C1i, Figure 4);

the fourth combining unit combining the external signal with a fourth predistorting coefficient (multiplier 55, coefficient C1q, Figure 4);

the fifth combining unit combining the in-phase component with a fifth predistorting coefficient (coefficient C0i, one of two multipliers in QGPA 36, Figure 3, column 6, lines 36-39);

the sixth combining unit combining the in-phase component with a sixth predistorting coefficient (coefficient C0q, one of two multipliers in QGPA 36, Figure 3, column 6, lines 36-39).

Regarding **claims 3 and 12**, Briffa et al. disclose everything claimed as applied to claims 2 and 11 above, and further disclose a second summer summing the outputs of first and third combining units (summer 57, Figure 4); and

a third summer summing the outputs of second and fourth combining units (summer 59, Figure 4).

Regarding **claims 4 and 13**, Briffa et al. disclose everything claimed as applied to claims 3 and 12 above, and further disclose a second multiplying unit which multiplies the output of the second summer with the in-phase component (one of two multipliers in QGPA 36, column 6, lines 36-39, Figure 3; it is implicit that the in-phase term of the predistortion signal p is multiplied by the in-phase branch of x; see also column 6, lines 9-36); and

a third multiplying unit which multiplies the output of the third summer with the quadrature component (other one of two multipliers in QGPA 36, column 6, lines 36-39, Figure 3; it is implicit that the quadrature phase term of predistortion signal p is multiplied by the quadrature phase branch of x), and wherein

the adder sums the outputs of the first combining unit, the sixth combining unit, the second multiplying unit and the third multiplying unit to produce a predistorted RF signal (summer of QGPA 36, column 6, lines 36-39; adjusted signal is output from QGPA 36 as signal r, column 6, lines 14-18, Figure 3).

Regarding **claims 17 and 18**, Briffa et al. discloses everything claimed as applied to claims 1 and 10, and further discloses the respective predistorting coefficients are provided to the combining unit from a microcontroller performing a search algorithm (the coefficients C of the predistortion signal are adjusted by the Controller 40 which adjusts the predistortion coefficients

by minimizing an error signal e (search for minimum error); controller 40 implemented with a microprocessor, column 6, line 55-column 7, line 13; Fig. 3)

6. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Briffa et al. (US 6,075,411) in view of Johnson et al. (US 5,577,236).

Regarding **claim 5**, Briffa et al. disclose everything claimed as applied to claim 1 above, but fail to expressly disclose the apparatus is an application specific integrated circuit (ASIC).

However, ASICs are well known in the art to reduce circuit size, decrease performance variations, and reduce the distance between circuit components, as evidenced by Johnson et al. (column 5, lines 25-29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the apparatus as applied to claim 1 as an ASIC since ASICs are well known in the art to reduce circuit size, and decrease performance variations.

7. **Claims 6 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Briffa et al. (US 6,075,411) in view of Giardina et al. (US 2003/0063686).

Regarding **claims 6 and 14**, Briffa et al. disclose everything claimed as applied to claims 1 and 10 above, but fail to expressly disclose an output carrying the X^2 signal is coupled to a delay unit and the output of the delay unit is fed back into the apparatus as the external signal, whereby the external signal is a delayed signal derived from the X^2 signal.

Giardina et al. teaches a predistortion model (page 3, equation 3, [0022]; Fig. 3; the u_{n-1} term refers to a delayed/previous signal sample, and in the case of k = 1, would produce a delayed "X^2" term). This predistortion circuit can produce predistortion based on current and

past input samples of the input signal using a relatively simple and low cost implementation (page 2, [0020]).

Therefore, it would have been obvious to one of ordinary skill in the art to provide Briffa et al. with the predistortion model taught by Giardina et al. since it is simple and cheap to implement. Furthermore, both Briffa et al. and Giardina et al. both teach predistortion, a common field of endeavor. Thus, Briffa et al. and Giardina et al. disclose the claimed invention except for the exact structure of the X2 output is coupled to a delay unit, and the output delay is fed back into the apparatus as the external signal. It would have been an obvious matter of design choice to specify such a design, since applicant has not disclosed that this specific structure solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well if implemented according to the model taught in Giardina et al. (page 3, equation 3).

8. **Claims 7, 9 and 15** rejected under 35 U.S.C. 103(a) as being unpatentable over Briffa et al. (US 6,075,411) in view of Wright et al. (US 2002/0044014).

Regarding **claims 7 and 15**, Briffa et al. disclose everything claimed as applied to claims 1 and 10 above, but fail to expressly disclose the apparatus and method comprising a further multiplier, which squares the X^2 signal again to give a X^4 signal, wherein the external signal is the X^4 signal.

Nevertheless, Briffa et al. suggests using higher order IMD terms my indicating the predistortion circuit can be implemented in any system for which third and higher order IMD compensation is desirable (column 7, lines 37-41; see also column 5, lines 3-7).

Wright et al. discloses the fourth order term (Figure 8, X^4) connected to a summer via DCSP 52 (digital compensation signal processor) with an FIR filter which permits compensation of a significant range of amplifier nonlinearity effects (page 9, [0196], Figure 8). Furthermore, Wright et al. teach that the 2nd order kernel is generated by squaring the x(t) signal (as depicted in Figure 6A).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to provide the circuit taught by Briffa et al. with the DCSP 52 taught by Wright et al. for compensation of a significant range of amplifier nonlinearity effects and increased control over weak non linear effects (pages 8-9, [0196]), and both Briffa et al. and Wright et al. suggest implementations for third or higher order IMD compensation is desirable. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate the squaring structure of x(t) for $x^2(t)$ since it has been held that mere duplication of essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Regarding **claim 9**, Briffa et al. disclose a feed forward amplifier arrangement comprising:

a compensating apparatus as claimed in claim 1 (PreD 37 and QGPA 36, Figures 3 and 4, see rejection of claim 1 above);

an amplifier (RF PA 13, Figure 3) having non-linear transfer characteristics that distort signals amplified thereby (column 5, lines 3-7; column 7, lines 20-22), the amplifier being coupled to the output of a compensating apparatus (QGPA 36, Figure 3);

a controller (40, Figure 3) which generates coefficients for feeding into the compensating apparatus (PreD 37, Figures 3 and 4); and

However, Briffa et al. fail to expressly disclose a sampling means which samples an output signal from the amplifier and which feeds the sample back to the controller.

Nevertheless, Briffa et al. does disclose a feedback path from the output of RF PA 13 which is coupled to a delayed input signal and the difference between the two signals is input into controller 40 to adjust predistortion signal coefficients to minimize the error (column 6, line 55 to column 7, line 6; Figure 3).

Wright teaches a similar system which samples the power amplifier output in ADC 68, which is fed back to ACPCE 70 for correction of coefficients used by DCSP 52 (page 5, [0153], [0154], Figure 1).

Because both Briffa et al. and Wright et al. teach similar circuits and methods of correcting/compensating coefficients used in predistortion devices using a feedback path from an output of a power amplifier, it would have been obvious to one of ordinary skill in the art to substitute one feedback coefficient update scheme for another, for the obvious result of providing updates and corrections to coefficients used in predistortion devices.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID HUANG whose telephone number is (571)270-1798. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSH/dsh
1/12/2009
/David Huang/
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611